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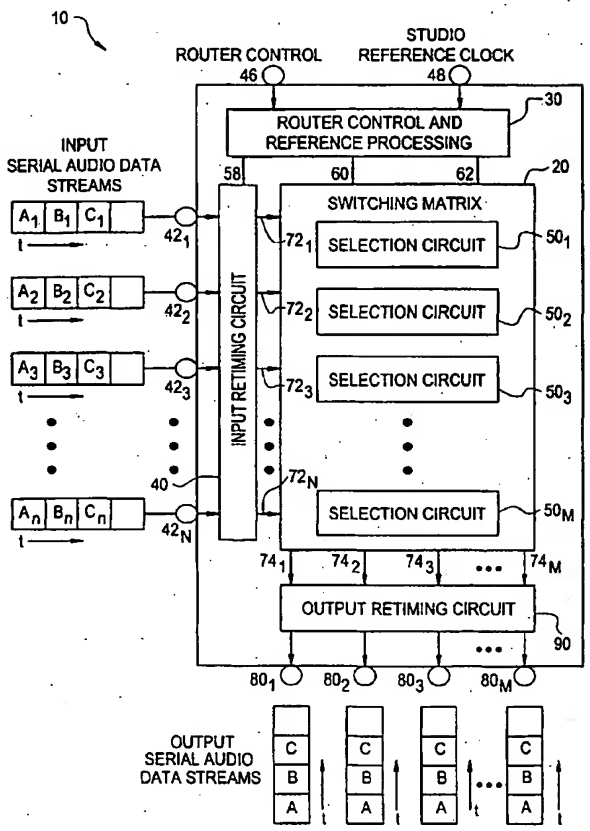
(54) Title: AUDIO ROUTER WITH CHANNEL BREAKAWAY



(57) Abstract: An apparatus (10) for independently routing channels from a plurality of serial, digital audio data streams to corresponding channels of a plurality of predetermined serial digital audio stream outputs. Apparatus according to the invention comprise a plurality of signal inputs (42_1, 42_2, 42_3,...42_N) for receiving serial audio data streams. Each audio data stream input may include two or more discrete channels of audio data with each input having the same number of channels. The apparatus also includes an input retiming circuit (40) to time-align corresponding channels of each input audio data stream and a switch (20) which accepts the plurality of time-aligned input data streams (72_1, 72_2, 72_3, ...72_N) and exclusively routes predetermined channels of predetermined inputs to corresponding channels of predetermined outputs (80_1, 80_2, 80_3, ...80_M).

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DESCRIPTION

AUDIO ROUTER WITH CHANNEL BREAKAWAY

Technical Field

The invention relates generally to audio routers. More particularly, the invention relates to an audio router that routes channels from one or more audio data streams independently to corresponding channels of one or more predetermined outputs.

Background Art

Audio routers are generally provided to connect any one of a number of audio signal inputs to any one of a number of audio signal outputs. The audio signals may be formatted in accordance with a number of audio signal standards. These standards consider analog or digital signals and whether the signals are single or multi-channel.

An audio router typically employs a type of switching matrix such as a crosspoint switch that allows for the connection of any one or more audio signal inputs to any one or more audio signal outputs. In an audio recording studio or a video studio environment, an audio router provides a necessary and complex function of input to output mapping that would otherwise require an exponential increase in the number of cables within the studio and a corresponding increase in the number of inputs and outputs on the primary audio and video devices employing such audio signals. In this fashion, an audio router allows signals to be switched, either statically or dynamically, to any one of a number of outputs.

Digital audio routers switch digital audio data streams that may be synchronous or asynchronous with one another. Since each digital audio stream input to a router may be generated by a different audio source, each audio stream will have a unique time or phase relationship. If the time relationships among inputs differ, the input audio data streams are asynchronous. If the time relationship among inputs is the same, the input audio data streams are synchronous. Whether the input audio data streams are synchronous or asynchronous, a digital audio router will typically time-align or re-clock each input to insure synchronism among all inputs.

Digital audio routers may provide additional functions related to the manipulation of the digital audio signals including signal inversion, signal amplitude modulation, simple signal summing and signal channel reversal. These functions may be performed with

respect to a known digital audio signal format such as the AES3 format specified by the Audio Engineering Society Incorporated.

The AES3 digital audio format uses a time division multiplexed, two channel, serial formatted digital audio data signal. Time division is a slotted communication technique in which each discrete stereo audio sample in time is assembled as a frame. Each frame comprises a first channel subframe and a second channel subframe. Within each subframe is a preamble that precedes and identifies the audio data that follows. The audio data and preambles each occupy a timeslot.

The first channel typically corresponds to the left channel of a stereo audio signal, and the second channel signal would correspond to the right channel. Within the audio frame, the left stereo channel signal subframe is followed in time by the right channel signal subframe. The serial digital audio data signal is therefore a multichannel signal, comprised of a sequence of preambles and audio data, each in consecutive time slots.

Serial digital signals can be routed from inputs to outputs by a conventional crosspoint switch. Such a switch connects any input to any output, and maintains this connection continually. Because the multiple channels of each serial data stream are channels on the same input, the channels of each input are necessarily directed to the same output.

Summary of the Invention

The present invention provides apparatus for independently routing channels from a plurality of serial, digital audio data streams to corresponding channels of a plurality of predetermined serial, digital audio stream outputs. Apparatus according to the invention comprise a plurality of signal inputs for receiving serial audio data streams. Each audio data stream input may include two or more discrete channels of audio data. All of the serial audio streams input have the same number of channels. The apparatus also includes an input retiming circuit to time-align corresponding channels of each input audio data stream and a switch which accepts the plurality of time-aligned input data streams and exclusively routes predetermined channels of predetermined inputs as they arrive at the switch to corresponding channels of predetermined outputs.

Another aspect of the present invention provides methods of independently routing channels from a plurality of audio data stream sources to corresponding channels of a

plurality of predetermined serial, digital audio stream outputs. The methods comprise time-aligning the plurality of input audio data streams into time-aligned corresponding channels and switching between the plurality of time-aligned input data streams thereby exclusively routing predetermined channels of predetermined inputs to corresponding channels of predetermined outputs.

In one aspect the present invention provides a digital audio router that accepts a plurality of digital audio signals and assembles an output signal consisting of individual channel data selected independently from any one of the digital audio input signals.

Accordingly, it is an object of the invention to route channels belonging to a plurality of input data streams independently to corresponding channels of a plurality of predetermined outputs.

Other objects and advantages of the apparatus and methods will become apparent to those skilled in the art after reading the detailed description of the best mode.

Brief Description of the Drawings

FIG. 1 is a system block diagram of an audio router according to one embodiment of the present invention.

FIGs. 2A, 2B and 2C are temporal representations of digital audio signals according to one embodiment of the present invention.

FIG. 3 is a system block diagram of the selection circuit according to one embodiment of the present invention.

FIGs. 4A, 4B, 4C and 4D are input and output frame diagrams showing the operation of one embodiment of the present invention.

FIGs. 5A and 5B are circuit diagrams of one selection circuit used in one embodiment of the present invention.

Best Mode of Carrying Out Invention

FIGs. 1 and 3 show an overall block diagram of the digital audio router 10 according to a preferred embodiment of the present invention. Digital audio router 10 includes a switching matrix 20 and control and reference clock processing circuitry 30. The router has a plurality of inputs 42 and a plurality of outputs 80. The switching matrix 20 is comprised of a plurality of selection circuits 50_1, 50_2, 50_3, ...50_M (where the subscript indicates a discrete selection circuit m). Each selection circuit 50_m allows for any one of a plurality of

inputs 42_1, 42_2, 42_3, ...42_N (where the subscript indicates a corresponding input n) to be coupled to one specific output. The number of router 10 outputs 80_1, 80_2, 80_3, ...80_M desired for a configuration determines the number of selection circuits 50_1, 50_2, 50_3, ...50_M employed. One selection circuit 50_m is associated with each output 80_m. For example, selection circuit 50_1 is associated with output 80_1, whereas circuit 50_2 is associated with output 80_2, and so on. The number N of inputs 42_1, 42_2, 42_3, ...42_N does not have to equal the number M of outputs 80_1, 80_2, 80_3, ...80_M. The system may include any number of inputs N and outputs M. The digital audio router 10 also includes input retiming circuitry 40 coupled to the switching matrix 20 and to the control and reference processing circuitry 30.

The input retiming circuitry 40 is coupled to the plurality of digital audio inputs 42_1, 42_2, 42_3, ...42_N and accepts digital audio signals from a plurality of sources. The digital audio inputs may be AES/EBU XLR connectors for balanced (differential) sources, or BNC or RCA connectors for single-ended sources or other suitable multiwire, multipin connectors. Other similar external cabling connectors may be used. Similar external connectors are provided for the router outputs 80_1, 80_2, 80_3, ...80_M.

The control and reference processing circuitry 30 accepts a router control signal 46 and a reference clock signal 48 provided at input connectors to the digital audio router 10. The control and reference processing circuitry 30 is coupled to the switching matrix 20 and the input retiming circuitry 40 to provide control data signals 60 and clocking signals 62 to the switching matrix 20 and a retiming clock signal 58 to the input retiming circuitry 40.

The control and reference processing circuitry 30 accepts router control data from the router control input 46. The router control data is provided from other studio equipment or from a keyboard, control panel or other conventional input/output device. The router control data consists of control messages generated by a user. The control messages direct the operation of the digital audio router 10 by conveying information that allows a user to configure each selection circuit 50_m. Each selection circuit 50_m assembles a serial audio data stream from data in specific channels of the input audio streams at the inputs 42_1, 42_2, 42_3, ... 42_N, as further discussed below, and supplies that data stream for output 74_m.

While the aforementioned AES3 standard specifies a two channel, serial time multiplexed audio data stream, serial audio data streams having more than two channels can

be input and routed by the present invention. Each audio data stream input to the router 10 must have the same number of channels.

A typical control message may, for example, direct the router 10 to assign selection circuit 50_4 to assemble an output containing channel A_2 from a second digital audio signal input 42_2 and channel C_3 from a third digital audio signal input 42_3. The router 10 control signals 46 and messages may be provided in any one of a number of known studio messaging formats, including known personal computer networking messages as well as other messaging protocols. The studio reference input 48 is provided, if desired, to supply a global clock reference signal used by the audio studio to synchronize all studio equipment. In this regard, the global clock or studio reference signal is used to synchronize all digital and audio equipment to a particular standard clock so as to harmonize the operational equipment within the studio. All internal equipment clocks within the studio are typically derived from the studio reference clock so that synchrony between the various pieces of audio equipment may be achieved.

The input retiming circuitry 40 includes within it, for example, a Crystal® Semiconductor CS 8412 multi-standard digital data receiver, decoder and jitter filter. The retiming circuit 40 synchronizes the digital audio sources input to the router 10 via the digital audio inputs 42_1, 42_2, 42_3, ...42_N using the retiming clocking signal 58. The router 10 may alternatively synchronize all digital audio inputs 42_1, 42_2, 42_3 ... 42_N using one input as a reference and synchronize all others to that reference. For example, input one 42_1 may be used as the reference. Channel clocking signals 62 may alternatively be derived during input 42_1, 42_2, 42_3 ... 42_N signal channel synchronization. One method by which the retiming circuitry 40 accomplishes this is by delaying one or any number of input audio signals by different times so that all subframes of a specific channel (*i.e.*, channel A) are time-aligned at the retiming circuit 40 outputs 72_1, 72_2, 72_3, ...72_N for all input audio signals. All other channel subframes (*i.e.*, channels B, C, D, *etc.*) that follow will be in proper time-alignment across all inputs. The output of the retiming circuitry 40 is coupled to the switching matrix 20.

The operation of the retiming circuit 40 is shown in FIGs. 2A and 2B. FIG. 2A shows an example of two asynchronous, two channel audio data streams input to the router 10. A first digital audio data signal 102 input to the router 10 on a first digital audio signal

input 42_1 and a second digital audio signal 104 input to the router 10 on a second digital audio signal input 42_2. The input digital audio signals 102, 104 have a temporal relationship such that channel A_1 106 and channel B_1 108 subframes for the first signal 102 are not time-aligned with channel A_2 110 and channel B_2 112 subframes for the second signal 104. The X 114 and Y 116 timeslots indicate standard preambles for the A and B channel data timeslots respectively. The information contained in a respective channel's preamble is in a format specified by the particular digital audio signal standard.

The corresponding channel subframes for the first 102 and second 104 signals are not presented at the digital audio inputs 42_1, 42_2 at the same time. The retiming clock signal 58 provides a reference signal to the retiming circuitry 40 such that the first 102 and second 104 digital audio signals output from the retiming circuitry 40 are time-aligned as shown in FIG. 2B. The time-aligned audio signal data streams are output 72_1, 72_2, 72_3, ...72_N from the retiming circuitry and are coupled to the switching matrix 20 as shown in FIG. 1.

The switching matrix 20 is comprised of a plurality of selection circuits 50_1, 50_2, 50_3, ... 50_M, one for each output 80_m. An individual selection circuit 50_m is shown in FIG. 3. Each selection circuit 50_m has a plurality of time-aligned inputs 72_1, 72_2, 72_3, ...72_N matching the number N of router 10 inputs 42_1, 42_2, 42_3, ...42_N and one output 74_m dedicated to the particular one of the outputs 80_m associated with that selection circuit.

Each selection circuit 50_m is comprised of an input/channel selector 52_m, an input/channel address decoder 54_m, and an input/channel address switch 56_m. The input/channel selector 52_m accepts the time-aligned audio signals output from the retiming circuit 40. The selector 52_m switches between signal inputs depending upon a timed control signal output from the input/channel address switch 56_m.

The input channel address decoder 54_m receives an address data signal from the router control and reference processor 30. The address assignment signal 60 contains user input/channel assignment information for each selection circuit 50_m. The input/channel address decoder 54_m decodes the address assignment signal 60 and loads signal input addresses for each channel of the output from the selection circuit 50_m into an index or data store 53. The user knows *a priori* the number of channels in the audio data stream standard used in the particular system. The user determines which channels from which inputs he desires for a given output from a particular selection circuit 50_m. For example, if the input

audio data streams have three channels, A, B, C, the input/channel address decoder 54_m after decoding an assignment signal 60 generated by a user will create an index containing a designation of a particular input 42 for channel A. A designation of an input 42 for channel B, and a designation of an input 42 for channel C. The inputs designated for different channels can be the same or different. One or more of the designated inputs may be null, *i.e.*, one or more channels in the output may be designated as corresponding to none of the inputs 42. For the example shown in FIG. 4C, the address decoder 54_1 for selection circuit 50_1 would have a corresponding index relating channel A to input 1, channel B to input 2 and channel C to input 2. Each channel/input relationship is therefore exclusive to a selection circuit 50_m output 74_m. The input/channel address decoder 54_m may be implemented using a processor or discrete circuit elements, and the physical elements which hold the index 53 may be the outputs out of the decoder 54_m. That is, the decoder 54_m may continually supply signals for all of the input assignments.

The output of the input/channel address decoder 54_m is coupled to the input/channel address switch 56_m. The input/channel address switch 56_m is synchronized with the channel clock 62. When the channel clock 62 indicates that a particular channel is being clocked through the input/channel selector 52_m, the input/channel address switch 56_m routes the input designation for that channel from index 53_m to input/channel selector 52_m. The input/channel 52_m selector connects the particular input denoted by that designation to the output 74_m of the selection circuit 50_m.

For example, if the input/channel address assignment signal 12 supplied to a particular selection circuit 50_m specifies input 72_3 for channel A, input 72_{10} for channel B and input 72_8 for channel C, the decoder 54_m of that selection circuit will place data designating these channels in store 53_m. When the channel clock 62 indicates that channel A is being clocked from input 72_3 into the input/channel selector 52_m, input/channel address switch 56_m will send the designation associated with channel A from store 53_m to the input/channel selector 52_m. This data designates input 72_3 to the output 74_m of selection circuit 50_m.

When the channel clock 62 indicates that channel B is being clocked, input/channel address switch 56_m supplies the designation associated with channel B from store 53_m, and hence input/channel selector 52_m connects input 72_{10} to output 74_m. When clock 62 indicates

channel C is being clocked through, input/channel address switch 56_m supplies the designation associated with channel C and input/channel selector 52_m connects input 72_8 to output 74_m.

Each selection circuit 50_m performs a switching action between router 10 inputs 72_1, 72_2, 72_3, ...72_N. The switching action allows for serial, time-aligned, channel audio data to be routed to the output 74_m independently of its associated input audio data stream. As described above, a user predetermines an output signal channel assignment for each selection circuit 50_m output 74_m. Each selection circuit 50_m output 74_m assignment assigns a particular channel (A, B, C, ...) from a particular serial audio data stream input (72_1, 72_2, 72_3, ...72_N) to occupy a corresponding channel timeslot of the output 74_m. Each channel/input assignment is exclusive.

As a general example of the selection circuit 50_m operation, FIGs. 4A, 4B, 4C and 4D illustrate the operation of two selection circuits 50_1, 50_2 of the present invention where the router 10 has two signal inputs 42_1, 42_2. These examples show two frames of audio data input to the router 10 where each frame is comprised of three subframes for channel A, B, and C data where a subscript identifies the input. For these examples, channel preambles will be ignored. As discussed above, a user configures each selection circuit output according to an input/channel assignment. The configurations are made to each selection circuit 50_m of the router 10 via the router control 46.

In FIG. 4A, the user specified an output 74_2 frame assignment for selection circuit two 50_2 (output 2) to only contain channel C_2 from input 2. No output 74_1 frame assignment for selection circuit one 50_1 (output 1) was made. There is no audio output from output 1. Output 2 only has audio data for channel C_2 of input 2. Channels A and B of output 2 are silent.

In FIG. 4B, the user specified an output 74_1 frame assignment for selection circuit one 50_1 (output 1) to contain channels B_2 and C_2 from input 2, and for selection circuit two 50_2 (output 2) to only contain channel C_2 from input 2.

In FIG. 4C, the user specified an output frame assignment for selection circuit one 50_1 (output 1) to contain channel A_1 from input 1 and channels B_2 and C_2 from input 2, and for selection circuit two 50_2 (output 2) to contain channel A_1 from input 1 and channel C_2 from input 2.

In FIG. 4D, the user specified an output frame assignment for selection circuit one 50_1 (output 1) to contain channel A_1 from input 1 and channels B_2 and C_2 from input 2, and for selection circuit two 50_2 (output 2) to contain channels A_1 and B_1 from input 1 and channel C_2 from input 2.

Each selection circuit 50_m allows for the routing of any combination of input audio data stream channels to corresponding channels of its output exclusively. Selection circuits 50_m do not allow for the combining or mixing of two or more of the same or different input audio stream channels into one channel timeslot of an output. Additionally, only corresponding input audio data channels can occupy corresponding selection circuit 50_m output channel timeslots. As the operational examples in FIGs. 4A-4D illustrate, only A channels input can occupy A channels output. The same applies for other channels in the input audio data streams. Additionally, each audio data stream input must have the same number of channels to properly time-align.

The channel clock 62 may be of any signaling format or logic level to indicate to the input/channel address switch 56_m when to direct the input/channel selector 52_m to switch from one time-aligned input 72_1, 72_2, 72_3, ...72_N to another. The switching between inputs 72_1, 72_2, 72_3, ...72_N is performed during the preamble timeslots to prevent audio data corruption. Corruption of the channel preambles can therefore occur. However, this information is discarded and regenerated during output retiming 90.

The timing relationship for switching between time-aligned inputs 72_1, 72_2, 72_3, ...72_N is illustrated in FIG. 2C. In the two input, two-channel example of FIGs. 2A-2C, the channel clock signal 62 discussion with reference to FIGs. 1 and 3 is in the form of a leading-edge/trailing-edge clock signal 282. This signal is synchronized with the time-aligned inputs 72_1, 72_2, 72_3, ...72_N such that the leading-edge and trailing-edge transitions are executed during channel preamble 114, 116 timeslot periods 290. For the clock signal 282 format illustrated in FIG. 2C, the input/channel address switch 56_m of each selection circuit 50_m is triggered to switch between channels by leading-edge transitions and trailing-edge transitions, rather than by the discrete logic levels in the signal. FIG. 2C illustrates the data coupling for a particular output from a particular selection circuit 50_m. In this example, the leading-edge and trailing-edge transitions direct the input/channel selector 52_m to couple

data from input 1 to the output during the channel A timeslot and to couple data from channel 2 to the output during the channel B timeslot.

Returning to FIG. 1, the output 74_m of each selection circuit 50_m from the switching matrix 20 is coupled to an output retiming circuit 90 for generating new channel preambles. The output retiming circuit 90 uses, for example, a Crystal® Semiconductor CS8402 transmitter to generate new audio channel preambles 292, 294 for each respective preamble timeslot. The retiming circuit 90 knows, *a priori*, the audio standard of the original signals input to the router 10 and generates new preambles for each channel preamble according to that standard. The output retiming circuitry 90 additionally insures that all router 10 outputs 80_1, 80_2, 80_3, ...80_M are synchronized.

FIGs. 5A and 5B show a two channel selection circuit 50_m embodiment using discrete digital circuitry. Each of the plurality of selection circuits 50_m would comprise the same circuitry shown in FIGs. 5A and 5B. The multiplexing circuitry shown in FIG. 5A constitutes a single input/channel selector 52_m. As discussed above, the digital audio signal inputs 72_1, 72_2, 72_3, ... 72_N discussed above are provided on a 64 channel parallel bus at 202 and fed to multiplexing circuitry 204. In the particular example of FIG. 5A, 64 such inputs are provided, *i.e.*, N equals 64. The inputs are distributed among multiplexer blocks 206, 208, 210 and 212. The lowest two bits of address data 220 are provided to select inputs for each of the multiplexers 230 to select one of four of the unique source audio inputs to those multiplexer units. The digital audio signals selected by the first level multiplexers are then fed to a second level multiplex unit 232 within each of the multiplexer blocks 206, 208, 210, 212. Address data 222 are provided as selection inputs for each of the multiplexers 232 to select one of the four first level signal selections. The digital audio signals selected by the second level multiplexers are then fed to a third level multiplexer 236. The next lowest two bits of address data 224 are then used to select a single digital audio data signal and provided for output as signal 240, which corresponds to the output 74_m of the selection circuits discussed above. Output signal $240/74_m$ is connected through retiming circuit 90 to one digital audio signal output 80_m of FIG. 1.

FIG. 5B illustrates an implementation of an input/channel address decoder 54_m, index store 53 and an input/channel address switch 56_m as discussed above. The control signal 60 discussed above is provided by control and reference processing circuitry 30 in the form of

left source addresses and right source addresses on busses 250 and 260 respectively. A left strobe 252 is also provided as part of the control signal 60 from the control and reference processing circuit 30 and provides a leading-edge clock to first level left strobe latches 254. Similarly, a right strobe 262 is provided as part of the control signal 60 from the control and processing circuitry 30 and provides a leading-edge clock to first level right strobe latches 264. These rising clock edges cause the left and right source addresses to be latched into left and right strobe latches 254 and 264 respectively. The latched left and right source addresses are presented to second level right and left latches 256 and 266 respectively. A reference signal 270 derived from studio reference 48 is provided as a clock to both right and left second level latches 256 and 266 and is also provided as part of the control signal 60. Once latched in the left and right second level strobe latches, 256 and 266 respectively, the second level latch data is presented to two input multiplexer block 274. Thus, the second level latches 256 and 266 act as the store 53 for the index discussed above. Latches 256 hold a designation for a particular input associated with the left or A channel output of the selection circuit, whereas latches 266 store the designation of a particular input associated with the right or B channel output of the selection circuit. Multiplexers in block 274 act as the input/address channel switch 56_m discussed above. Channel clock 60 discussed above is provided as an enabling input 280 to the multiplexers within multiplexer block 274 to select between the latched source addresses from either the left channel latches 256 or the right channel latches 266. When the channel clock is high, the left source address data from the second level left strobe latches is presented at outputs 276 of multiplexer block 274. When the channel clock is low, the data from second level right strobe latches 266 is presented at outputs 276 to multiplexer block 274. Outputs 276 include address lines 220, 222 and 224 of FIG. 5A so as to provide either the left source address from latches 256 or 261 to the multiplexing circuitry 204. Thus, the alternating phases of the channel clock cause the input digital audio signal identified by the source address to be provided on output signal 240 for output at digital audio output 80.

The timing relationship for the presentation of the selected input digital audio signal previously discussed in FIG. 2C is applicable. In this regard, channel clock 282 on channel clock signal 280 is shown as a high when presenting the output digital data 242 on output signal 240 as A_1 from signal 102 and after passing through the circuitry on FIGs. 5A and 5B

to signal output 74_m. When channel clock 282 is low, the B_2 channel data from signal 104 is presented at output signal 240 and thereon to signal output 80.

Also as shown in FIG. 2C, the channel clock transitions between high and low within a timing window 290 surrounding the preambles for the channel data 114 and 116. Ensuring a proper set of time 291 to the end of the preamble 292 will ensure that the selection circuitry within switch 20 in FIGs. 5A and 5B have sufficient time to present the output digital audio data signal 240 to the signal output 80_m after calculation through multiplexer circuit 204 without corruption of that data. Furthermore, output retiming circuitry 90 may be used to regenerate first and second channel preamble data 292 and 244 for channels A and B since the transitioning of the multiplexer circuitry 204 within FIGs. 5A and 5B will corrupt that data at signal output 80_m without such preamble regeneration.

In an alternative embodiment of the present invention, the input audio signals are synchronized by the input retiming circuitry 40 and provided as synchronized digital audio data streams 72_1, 72_2, 72_3, ...72_N, but the preamble data is removed from the digital signals. The synchronization or retiming is performed as described above. Such preamble stripping may, for example, be desired if the digital audio signals arrive in different digital audio formats or if the input audio signals are of mixed digital formats. In this embodiment, the switching matrix 20 operates as described above to create an output digital data stream comprising of audio data from different channels of different input audio signals, but further processing is provided by the output retiming circuitry 90 shown in FIG. 1.

The output retiming circuitry 90 operates substantially as described above with respect to input retiming circuitry 40 to generate the channel preambles. The output retiming circuitry 90 insures that all output signals 74_1, 74_2, 74_3, ...74_M are synchronized from the plurality of selection circuits 50_m and regenerates the necessary preamble data within the output digital audio signal as needed for the equipment connected to the audio outputs 80_1, 80_2, 80_3, ...80_M.

The output retiming circuit 90 allows for audio router applications in which an audio standard needs to be regenerated after a signal 74_m exits a selection circuit 50_m. One example of this includes digitized analog audio input provided at a router input 42_n and that are provided with no preamble since the input audio data format is unknown. Thus the

output retiming circuit 90 generates new preamble data for the output audio signals provided on the router outputs 80_1, 80_2 80_3, ...80_M.

Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

Industrial Applicability

The present invention is useful, *inter alia*, in the sound recording and broadcast

Claims:

1. An audio router (10) characterized by:

a plurality of signal inputs (42_1, 42_2, 42_3, ...42_N), each said input adapted to receive a serial audio data stream, each said serial audio data stream including audio data for at least two channels and all of said audio data streams input having the same number of channels;

a plurality of signal outputs (80_1, 80_2, 80_3, ...80_M), each said output adapted to output a serial audio data stream having a said same number of channels; and

a switching matrix (20) adapted to couple one or more channels of one or more of said input serial audio data streams independently to corresponding channels of one or more serial audio data streams output from said plurality of signal outputs (80_1, 80_2, 80_3, ...80_M) whereby each channel of an output serial audio data stream may be coupled to the corresponding channel of an input serial audio data stream.

2. The audio router (10) of claim 1 wherein said switching matrix (20) is further characterized by a selection circuit (50_m) associated with each one of said plurality of signal outputs (80_1, 80_2, 80_3, ...80_M).

3. The audio router (10) of claim 2 is further characterized by:

a control and reference processor (30) adapted to receive a router control signal (46) and a reference clock signal (48), said control signal (46) includes control messages specifying input/channel address assignments (60) for each said selection circuit (50_m).

4. The audio router (10) of claim 3 is further characterized by:

an input retiming circuit (40) coupled to said plurality of signal inputs (42_1, 42_2, 42_3, ...42_N) and said switching matrix (20), said input retiming circuit (40) time-aligns each serial audio data stream input to said router (10) whereby said channels belonging to each respective serial audio data stream input time-align with all other corresponding serial audio data stream channels input; and

said time-aligned serial audio data streams (72_1, 72_2, 72_3, ...72_N) are input to said switching matrix (20).

5. The audio router (10) of claim 4 wherein each said selection circuit (50_m) is further characterized by:

an input/channel selector (52_m) to couple one of said time-aligned serial audio data streams (72_1, 72_2, 72_3, ...72_N) to an output (80_m);

an input/channel address decoder (54_m) adapted to accept an input/channel address assignment (60) including a plurality of channel designations each denoting one input (72_n) or no input, each such channel designation being associated with one channel in the input and output data streams;

an input/channel address switch (56_m) adapted to receive a channel clock signal (62) indicating at what time a particular channel is present at said input/channel selector (52_m), said input/channel address switch (56_m) being coupled to said input/channel address decoder (54_m) and said input/channel selector (52_m); and

said input/channel address switch (56_m) being operative to deliver the channel designation associated with a particular channel when that channel is present at the input/channel selector (52_m), said input/channel selector (52_m) being operative to switch between said plurality of time-aligned serial audio data streams (72_1, 72_2, 72_3, ...72_N) depending on the channel designation delivered by the input/channel address switch (56_m), whereby a serial audio data stream output (74m) is assembled from channels obtained from said time-aligned serial audio data stream (72_1, 72_2, 72_3, ...72_N) channels in accordance with the address assignment (60) provided to the selection circuit (50_m).

6. The audio router (10) of claim 5 wherein said audio data stream channel data includes a preamble (114, 116) for each sample of respective channel audio data (106, 108), each said channel preamble (114, 116) occupying a period of time (290), the router (10) is further characterized by said input/channel address switch (56_m) causing said input/channel selector (52_m) to switch between said plurality of time-aligned serial audio data streams (72_1, 72_2, 72_3, ...72_N) during said channel preamble period (290) so as to prevent corruption of said respective channel audio data (106, 108).

7. The audio router (10) of claim 6 is further characterized by:

an output retiming circuit (90) coupled between said selection circuit (50_m) outputs (74_m) and said outputs (80_1, 80_2, 80_3, ...80_M) of the router (10) for generating said channel preambles (114,116).

8. A method of assembling a serial audio data stream output from a plurality of serial audio data stream inputs, said serial audio data stream inputs and output having the same number of audio data channels, said method characterized by:

providing at a plurality of signal inputs (42_1, 42_2, 42_3, ...42_N) the plurality of serial audio data streams inputs;

selecting predetermined audio data channels independently from the plurality of serial audio data streams as the channels of the plurality of serial audio data streams are input; and

assembling the data in the selected channels to form the serial audio data output stream.

9. The method of claim 8 is further characterized by:

time-aligning (40) said serial audio data streams from said plurality of signal inputs (42_1, 42_2, 42_3, ...42_N) to provide time-aligned serial audio data stream inputs (72_1, 72_2, 72_3, ...72_N) having corresponding channel data for each aligned-in-time with each other.

10. The method of claim 9 is further characterized by:

providing a reference clock signal (48), said time-aligning step providing said time-aligned serial audio data steam inputs in synchronism with said reference clock; and

providing a channel clock (62) in synchronism with said reference clock signal (48), whereby said step of selecting predetermined audio data channels being perform in synchronism with said channel clock (62).

11. The method of claim 10 wherein each said serial audio stream channel includes a preamble (114, 116) for each sample of respective channel audio data (106, 108), each said channel preamble (114, 116) occupying a period of time (290), the method being further characterized in that said step of selecting channels includes switching between said plurality of time-aligned serial audio data streams (72_1, 72_2, 72_3, ...72_N) during said channel preamble periods (290) so as to prevent corruption of said respective channel audio data (106, 108).

12. The method of claim 11 further characterized by:

generating channel preambles (90) for the assembled serial audio data stream.

13. The method of claim 12 further characterized by providing control messages to control said step of selecting predetermined audio data channels independently from the plurality of serial audio data streams.

14. An audio router (10) characterized by:

a first signal input (42_1) and a second signal input (42_2), each signal input receiving an audio data stream in a serial format, said serial format including first channel data and second channel data;

a signal output (80_1) for outputting an audio data stream (240) in said serial format; and

a crosspoint matrix (20) electrically connecting said first signal input (42_1) and said second signal input (42_2) to said signal output (80_1), said crosspoint matrix (20) including a selection circuit (50_m) for selecting said first channel data for said output audio data stream (240) from said first channel data provided on one of said first and second signal inputs, said selection circuit (50_m) also selecting said second channel data for said output audio data stream (240) from said second channel data provided on said other of said first (42_1) and second (42_2) signal inputs.

15. The audio router (10) of claim 14 wherein said selection circuit (50_m) is further characterized by:

a latch circuit (254, 256, 264, 266) for latching a channel selection address, said latched channel selection address (276) providing a signal input identifier; and

a multiplexing circuit (204) electrically connecting said latching circuit (254, 256, 264, 266), each of said signal inputs (202) and said signal output (240), said multiplexing circuit (204) providing said audio data stream from said first or said second channel data on said signal output (240) according to said signal input identifier.

16. The audio router (10) of claim 15 wherein said latch circuit (254, 256, 264, 266) latches said channel selection address (276) according to a reference control signal (270) and said multiplexing circuit (204) is presented with said signal input identifier according to a channel clock (280).

17. The audio router (10) of claim 16 is further characterized by:

input retiming circuitry (40) electrically connecting said signal inputs (42_1, 42_2, 42_3, ...42_N) and said crosspoint matrix (20), said input retiming circuitry (40) clocking

out said audio data streams from said first and said second signal inputs according to a reference clock (58) so as to time-align all of said first channel data and said second channel data from said signal inputs with said reference clock (58).

18. The audio router (10) of claim 17 is further characterized by:

a control circuit (30) electrically connected to said input retiming circuitry (40) and said crosspoint matrix (20), said control circuit (30) having a router control input (46) and a reference clock input (48), said control circuit (30) producing said reference clock (58) and said channel clock (62) from a studio reference signal on said reference input (48), said router control input (46) providing control messages to said audio router (10) including said channel selection address (250, 260).

19. The audio router (10) of claim 18 wherein said first channel data and said second channel data include a first preamble and a second preamble respectively, said channel clock (62) changing state during said first and second preambles so as to prevent corruption of said output audio data stream.

20. The audio router (10) of claim 19 wherein said first and second preambles are regenerated by said output retiming circuit (90).

21. The audio router (10) of claim 14 wherein said serial format is the AES3 format.

22. The audio router (10) of claim 14 wherein said crosspoint matrix (20) includes 64 signal inputs (72_1, 72_2, 72_3, ...72_N) and 64 signal outputs (74_1, 74_2, 74_3, ...74_M), each of said signal outputs including said selection circuit (50_1, 50_2, 50_3, ...50_M).

23. A method of creating a digital output audio data stream in a serial format, said serial format including first channel data and second channel data, said method characterized by:

providing at a first signal input (42_1) an audio data stream in said serial format;

providing at a second signal input (42_2) an audio data stream in said serial format;

selecting (20) said first channel data for said digital output (80_1) audio data stream from said first channel data on one of said first and second signal inputs;

selecting (20) independently from said first channel data said second channel data for said digital output (80_1) audio data stream from said second channel data on one of said first and second signal inputs; and

outputting (80_1) said digital output audio data stream having said selected first and second channel data.

24. The method of claim 23 is further characterized by:

synchronizing (40) said audio data streams from said first (42_1) and second (42_2) signal inputs such that said first channel data and said second channel data are time-aligned.

25. The method of claim 24 is further characterized by:

providing a studio reference signal (270); and

deriving a channel clock (62) from said studio reference signal (270), said selection of said first channel data and said second channel data occurring on a transition of said channel clock (280).

26. The method of claim 25 wherein said first channel data said second channel data for said audio data streams further includes a first and a second preamble respectively, said method is further characterized by regenerating (90) said first and second preambles.

27. The method of claim 26 wherein said transition of said channel clock (62) occurs during said first and second preambles.

28. The method of claim 23 wherein said audio router includes a control circuit (30) and an input retiming circuit (40), said method further characterized by:

providing router messages to said control circuit (30);

providing a studio reference clock to said control circuit (30); and

deriving a reference clock (62) from said studio reference clock, said selection of said first channel data and said second channel data occurring on a transition of said channel clock.

29. An audio router (10) characterized by:

a first signal input (42_1) and a second signal input (42_2), each signal input receiving an input audio data stream, each audio data stream having first channel data and second channel data;

a signal output (80_1) for providing an output audio data stream (240), said output audio data stream having first channel data and second channel data;

a router control circuit (30) for accepting router control messages on a router control input (46) and providing first channel addresses (250) and second channel addresses (260) on control data signals;

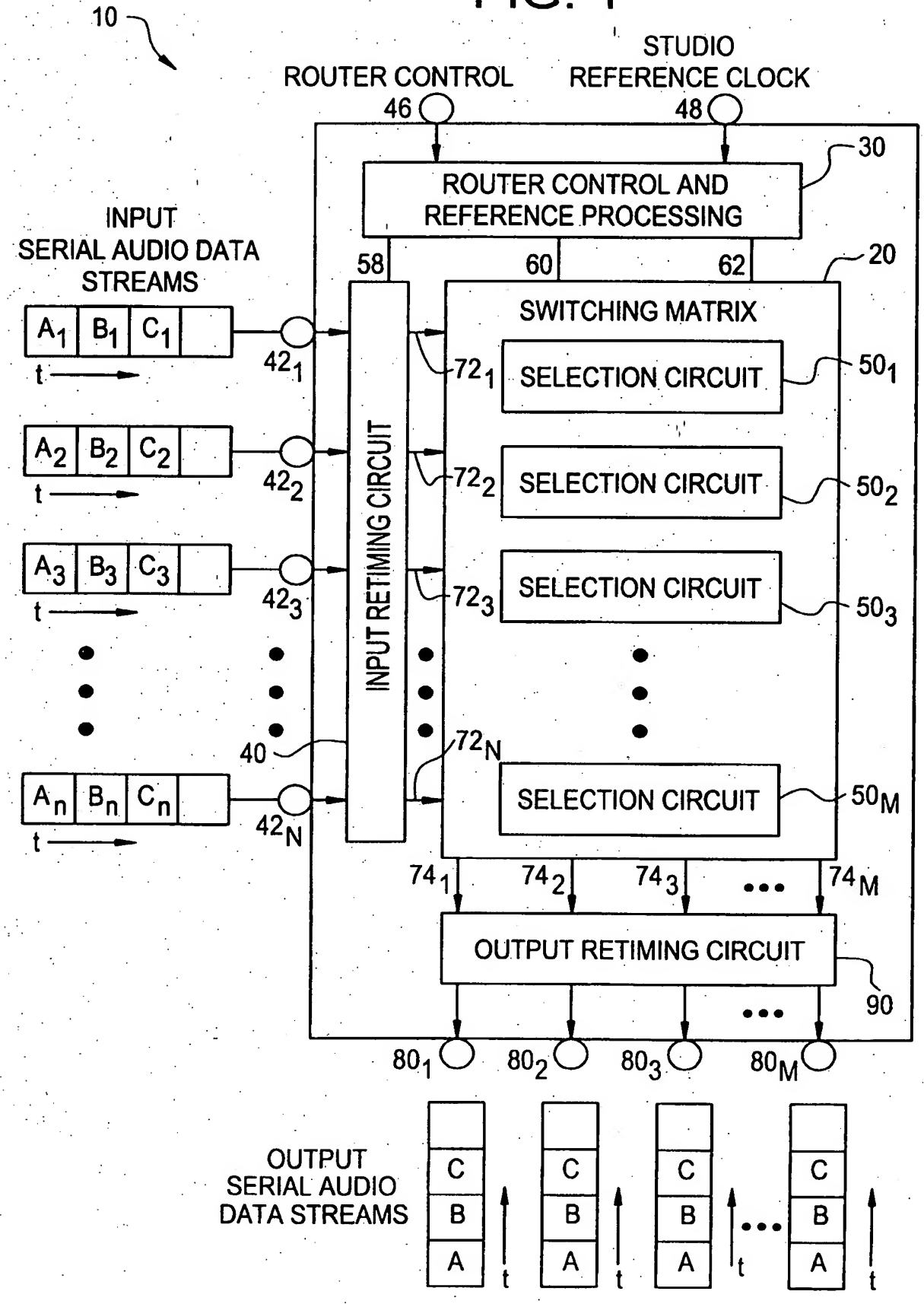
a reference generation circuit (30) for accepting a studio reference signal at a studio reference input (48) and providing a synchronization signal (58), a first channel strobe signal (252), a second channel strobe signal (262) and a channel clock (280) based upon said studio reference signal;

an input retiming circuit (40) electrically connecting said first signal input (42_1) and said second signal input (42_2) and accepting said synchronization signal (58), said input retiming circuit (40) synchronizing said audio data streams of said first signal input and said second signal input so as to output said first channel data and said second channel data for said first signal input and said second signal input simultaneously; and

a crosspoint matrix (20) electrically connecting said input retiming circuit (40), said control circuit (30), said router control circuit (30), said reference generation circuit (30) and said signal output (80_1), said crosspoint matrix (20) including a mulitiplexer circuit (204) and a channel address selection circuit, said channel address selection circuit accepting said first (250) and second (260) channel addresses, said first (252) and second (262) channel strobe signals, and said channel clock (280), said channel address selection circuit alternately outputting an audio input identifier (276) in response to said first channel address (250) clocked by said first channel strobe (252) or said second channel address (260) clocked by said second channel strobe (262), said channel identifier being alternately selected by said channel clock (280); said channel identifier used by said multiplexer circuit (204) to select one of said synchronized audio data streams from said first signal input (42_1) or said second signal input (42_2), said selected audio data stream providing said output audio data stream (240) on said signal output (80_1).

30. The audio router of claim 29 is further characterized by an output retiming circuit (90) for providing preamble information to said output audio data stream (240).

FIG. 1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ROUTER CONTROL
46
STUDIO
REFERENCE CLOCK
48
30
ROUTER CONTROL AND
REFERENCE PROCESSING
INPUT
SERIAL AUDIO DATA
STREAMS
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60
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SWITCHING MATRIX
INPUT RETIMING CIRCUIT
SELECTION CIRCUIT
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SELECTION CIRCUIT
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OUTPUT RETIMING CIRCUIT
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OUTPUT
SERIAL AUDIO
DATA STREAMS
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FIG. 2A

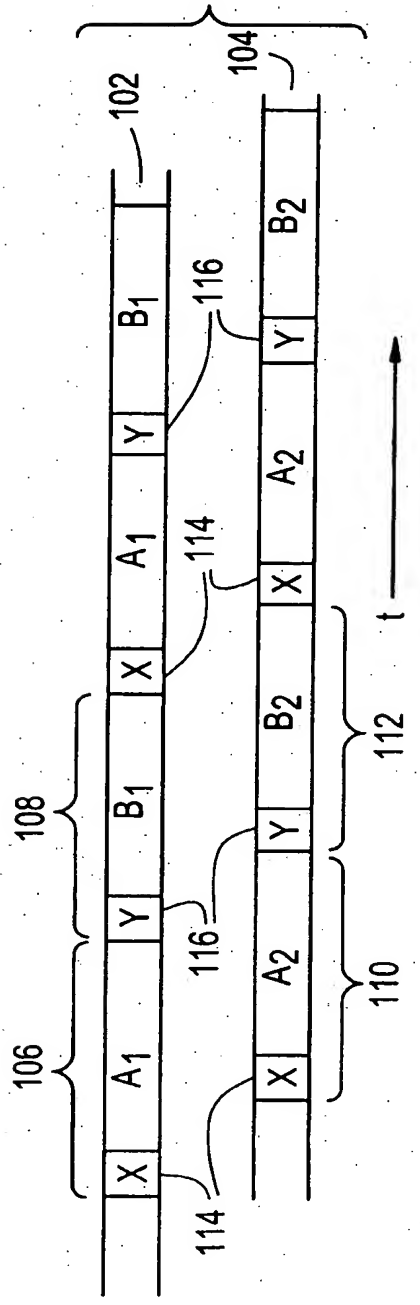


FIG. 2B

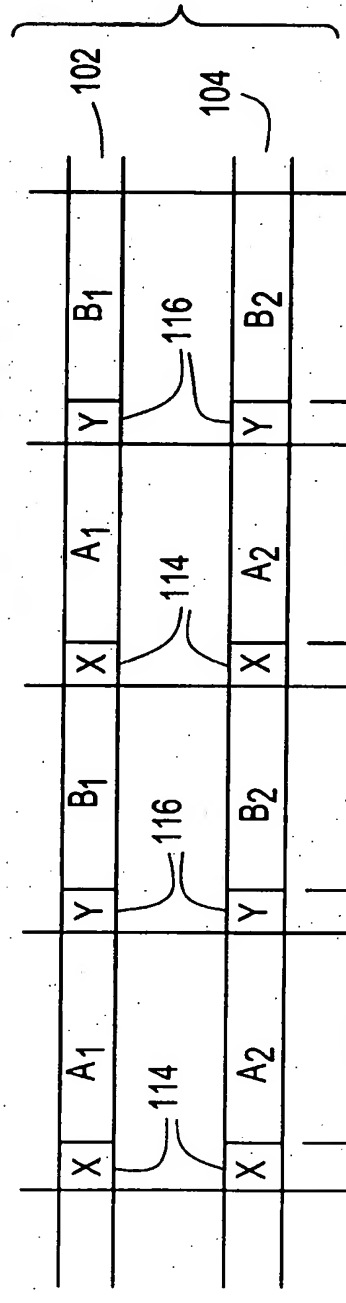
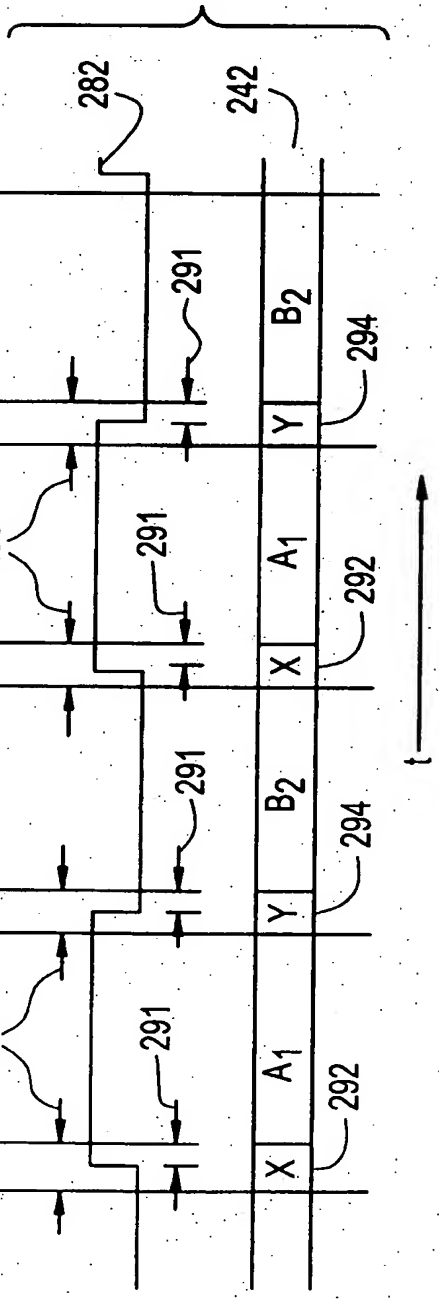


FIG. 2C



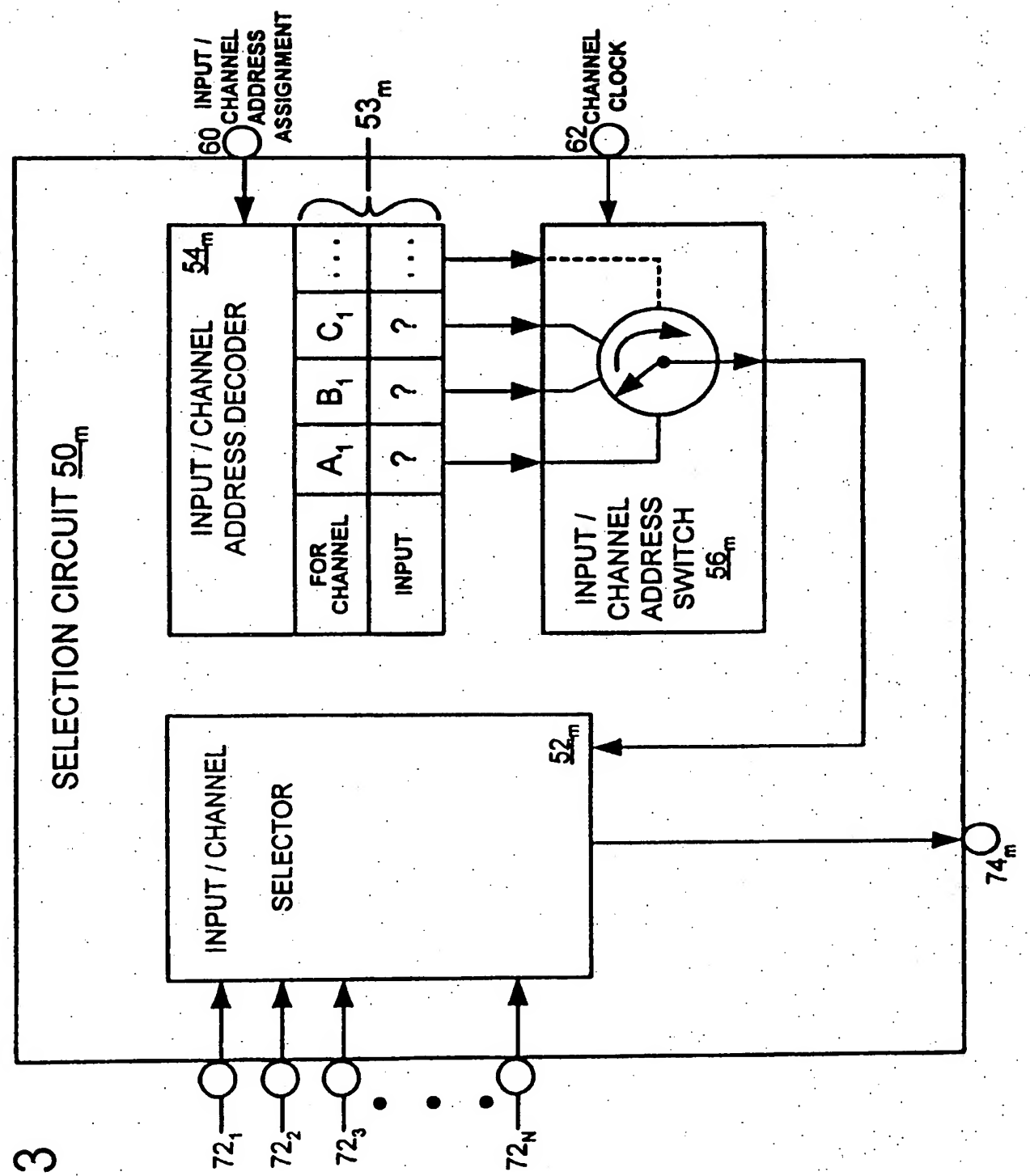

SELECTION CIRCUIT 50m
60 INPUT / CHANNEL ADDRESS ASSIGNMENT
53m
62 CHANNEL CLOCK
54m
INPUT / CHANNEL ADDRESS DECODER
FOR CHANNEL
INPUT
A1
B1
C1
?
?
?
INPUT / CHANNEL ADDRESS SWITCH 56m
52m
INPUT / CHANNEL SELECTOR
74m
72 1
72 2
72 3
72 N

FIG. 3

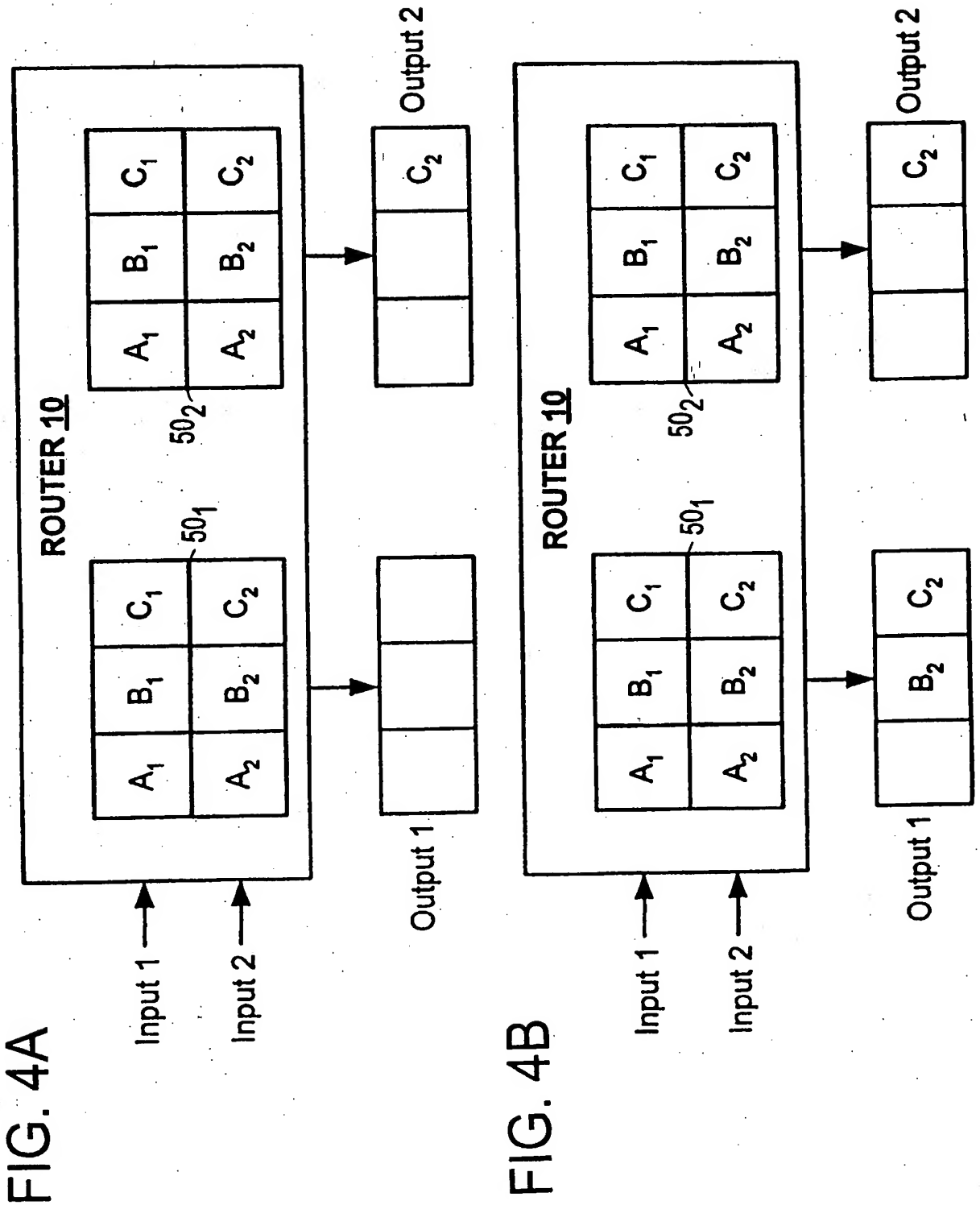

ROUTER 10
Input 1
Input 2
Output 1
Output 2
A_1 B_1 C_1
A_2 B_2 C_2
50_1
50_2

FIG. 4A

FIG. 4B

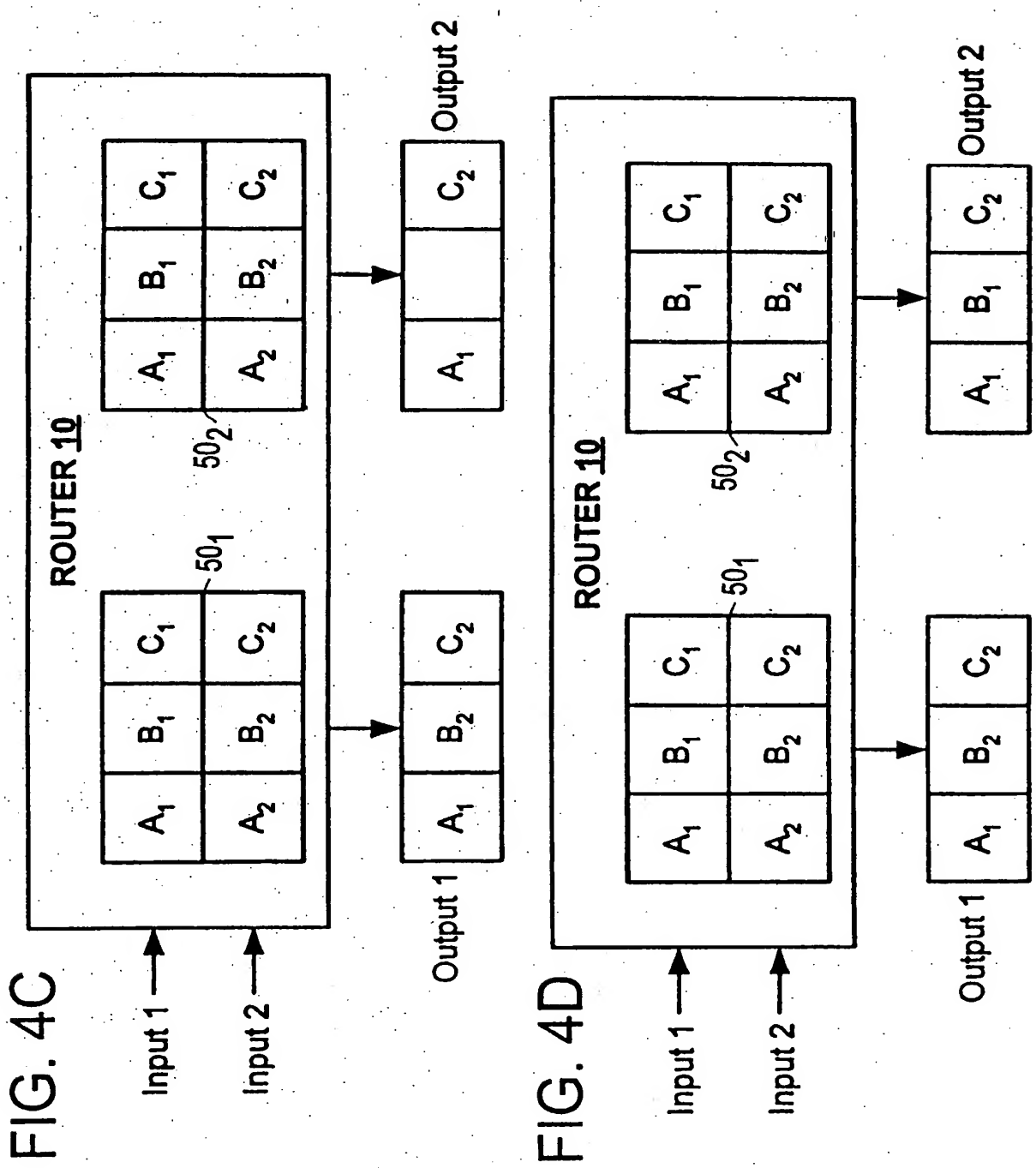
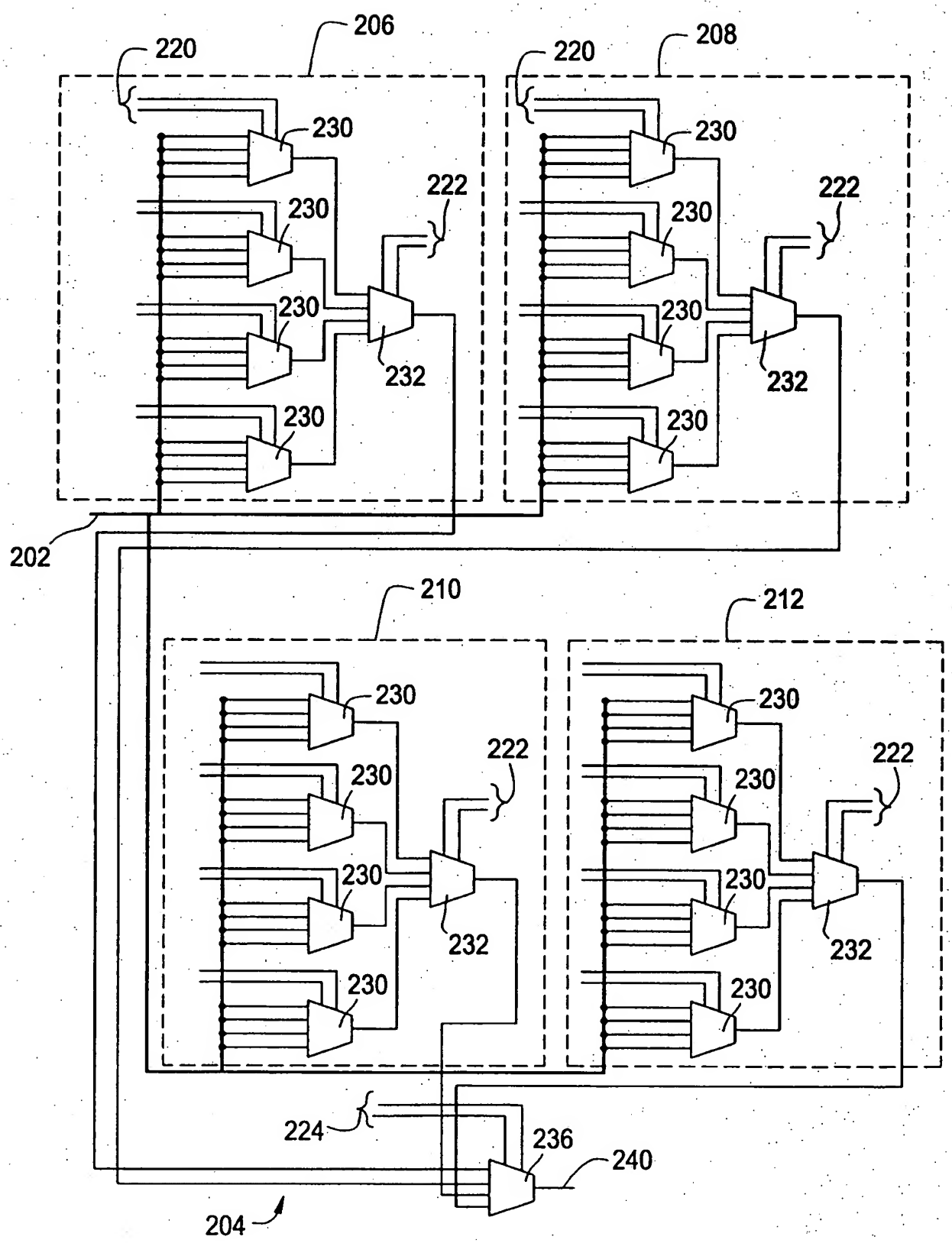

ROUTER 10
Input 1
Input 2
Output 1
Output 2
A_1 B_1 C_1 A_2 B_2 C_2
50_1
50_2

FIG. 4C

FIG. 4D

FIG. 5A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204

FIG. 5B